LISTING OF THE CLAIMS (1-42)

Claim 1 (original): A method for timestamping events in a primary event stream, the method comprising:

receiving the primary event stream;

distributing events in the primary event stream among a plurality of secondary event streams; and

timestamping events in each of the secondary event streams with a resolution of less than one clock cycle.

Claim 2 (original): The method of Claim 1 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

Claim 3 (original): The method of Claim 1 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

Claim 4 (original): The method of Claim 1 wherein the primary event stream is a differential signal.

Claim 5 (original): The method of Claim 1 wherein the secondary event streams are differential signals.

Claim 6 (currently amended): The method of Claim 1 wherein distributing events in the primary event stream comprises selectively enabling a plurality of gates such that a first event in the primary event stream [[is]] passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

Claim 7 (currently amended): The method of Claim 1 wherein distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary even stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

Claim 8 (currently amended): The method of Claim 1 wherein distributing events in the primary event stream comprises:

distributing rising edge events in the primary event stream among a first plurality of secondary event streams; and

distributing falling edge events in the primary event stream among a second plurality of secondary event streams.

Claim 9 (original): The method of Claim 1 further comprising:

registering the events in each of the secondary event streams.

Claim 10 (currently amended): A circuit for timestamping events with a resolution of less than one clock cycle in a primary event stream, the circuit comprising:

an event stream distributor coupled to receive the primary event stream; and

a plurality of timestamp circuits, each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor.

Claim 11 (original): The circuit of Claim 10 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

Claim 12 (original): The circuit of Claim 10 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

Claim 13 (original): The circuit of Claim 10 wherein the primary event stream is a differential signal.

Claim 14 (original): The circuit of Claim 10 wherein the secondary event streams are differential signals.

Claim 15 (original): The circuit of Claim 10 wherein the event stream distributor comprises:

a first counter coupled to receive the primary event stream; and

a first plurality of gates coupled to the first counter.

Claim 16 (original): The circuit of Claim 15 wherein the first counter is a Johnson counter.

Claim 17 (original): The circuit of Claim 15 wherein the first counter is an N-bit counter.

Claim 18 (original): The circuit of Claim 15 further comprising:
a second counter coupled to receive the primary event stream; and
a second plurality of gates coupled to the second counter.

Claim 19 (original): The circuit of Claim 10 further comprising:
a plurality of registers, each register operable to register events of one or more secondary event streams.

Claim 20 (currently amended): A method for timestamping events with a resolution of less than one clock cycle in a primary event stream, the method comprising:
receiving the primary event stream;
distributing rising edge events in the primary event stream among a first plurality of event streams;
recording an arrival time of each event in the first plurality of secondary event streams with respect to a reference clock with a resolution of less than one clock cycle;
distributing falling edge events in the primary event stream among a second plurality of event streams; and
recording an arrival time of each event in the second plurality of secondary event streams with respect to the reference clock.

Claim 21 (original): The method of Claim 20 wherein an event rate in each secondary event stream of the first plurality and the second plurality of secondary event streams is lower than an event rate in the primary event stream.

Claim 22 (original): The method of Claim 20 wherein the primary event stream is a differential signal.

Claim 23 (original): The method of Claim 20 wherein each secondary event stream of the first plurality and the second plurality of secondary event streams are differential signals.

Claim 24 (original): The method of Claim 20 wherein distributing rising edge events comprises selectively enabling a first plurality
of gates and distributing falling edge events comprises selectively enabling a second plurality of gates.

Claim 25 (original): The method Claim 20 wherein distributing rising edge events comprises selectively enabling a first plurality of gates using a first counter that is clocked by the primary event stream and distributing falling edge events comprises selectively enabling a second plurality of gates using a second counter that is clocked by the primary event stream.

Claim 26 (currently amended): A circuit for timestamping events with a resolution of less than one clock cycle in a signal, the circuit comprising:

a first counter coupled to receive the signal; and

a first plurality of gates, each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter.

A' (cont.)

Claim 27 (original): The circuit of Claim 26 wherein the first plurality of gates are AND gates.

Claim 28 (original): The circuit of Claim 26 wherein the signal is a differential signal.

Claim 29 (original): The circuit of Claim 26 wherein the signal is a single-ended signal.

Claim 30 (original): The circuit of Claim 26 wherein the first counter is a Johnson counter.

Claim 31 (original): The circuit of Claim 26 wherein the first counter is an N-bit counter.

Claim 32 (original): The circuit of Claim 26 further comprising:

a second counter coupled to receive the primary event stream; and

a second plurality of gates, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the seined counter.

Claims 33-42 (canceled)